SILICON LABS

Whitepaper

Simplifying FPGA Reference Clocking

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Field-Programable Gate Arrays (FPGAs) play a key role in numerous high-performance applications. They are widely used in data centers; industrial applications include broadcast video, print imaging, medical imaging, industrial control, cameras, conferencing and collaboration, digital signage, and many more.

Unlike earlier generations, current FPGAs require multiple reference clocks with precise frequencies (figure 1) that are not simply integer divisions of some base value. High-end FPGAs are system-on-chip (SoC) devices with bundled processing cores such as the ARM Cortex that have their own set of reference clocks; or they include embedded serializer/deserializers (SERDES) that have stringent jitter requirements to meet end applications' bit-error rate (BER) specifications.

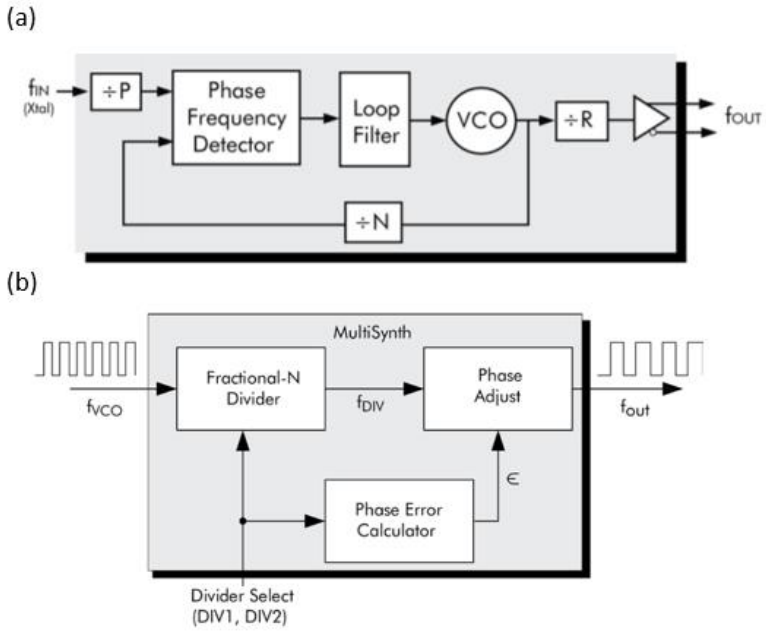
Component	Typical Reference Clock (MHz)
Processor/Network Processors	33.33, 66.66, 100, 125, 133.33
Memory	100, 133, 166, 200, 266
Fast Ethernet	25
Gigabit Ethernet	106.25
Fibre Channel	100
PCI Express 2.0	100

xDSL	35.328, 70.656
SONET/SDH OC-3/STM-1	77.76
SONET/SDH OC-12/STM-4	155.52
HD-SDI	74.1758, 74.25
3G-SDI	148.3517, 148.5
T1	1.544
E1	2.048

Table 1: Some of the reference clock frequencies seen by high-end FPGA-based systems

A New Approach is Needed for Clock Reference Architectures

Implementing a complex clock tree while still meeting severe space restrictions and a compressed time-to-market requires a new approach to clock generator design. The traditional architecture, shown below (a), is based around a simple integer-N phase-locked loop (PLL) that generates a voltage-controlled oscillator (VCO) output at a multiple of the desired frequency; the VCO feeds a divide-by-R block that produces the final output.



A comparison of (a) the traditional PLL and (b) the MultiSynth clock generation architectures

In this architecture, the output clock frequency is a function of the input clock frequency and the PLL divider values as shown:

$$f_{out} = \frac{f_{in} \bullet N}{P \bullet R}$$

A traditional single PLL-based architecture is suitable for simple integer clock multiplication of reference inputs or clock generation from a crystal input. However, high-end FPGAs require multiple non-integer-related frequencies: the crystal frequency must be changed to support each unique frequency plan. The designer must use one or more custom crystals and multiple clock generator ICs to generate the required set of frequencies, increasing the cost, complexity and power consumption of the overall solution.

Silicon Labs' patented MultiSynth™ fractional divider architecture, shown in Figure 2(b), solves this problem. The MultiSynth architecture replaces the divide-by-R block in 2(a) with a fractional-N divider that switches seamlessly between the two closest integer divider values to produce the exact output clock frequency with zero ppm error.

This process generates phase error: to eliminate it, the MultiSynth block calculates the relative phase difference between the fractional-N divider clock and the desired output clock and dynamically adjusts the phase to match the ideal clock waveform.

This technique makes it possible to generate any output clock frequency without sacrificing jitter performance.

Silicon Labs Timing Solutions

The Multisynth architecture is put to good use in Silicon Lab's portfolio of timing solutions, which includes the industry's broadest portfolio of crystal oscillator, clock generator, clock buffer, and jitter attenuator families.

	Oscillators	Clock Gems	JA Clocks
<100fs RMS	Si54x	Si5391	Si539x
100-200fs RMS		Si5341/0	Si534x
200-500fs RMS	Si53x	Si5332	Si532x
500-800fs RMS	Si59x Si51x	Si5338	
>1ps RMS		Si5351/0	

The Silicon Labs timing solution portfolio combines frequency flexibility with best-in-class jitter performance

Clock generators or jitter-attenuating clocks can supply up to 12 outputs with a maximum frequency of 1028 MHz and a typical jitter as low as 69 fs RMS. A range of output types is supported, including LVPECL, LVDS, HCSL, CML, and LVCMOS.

The table above shows an overview of the portfolio organized by jitter performance level: the parts at the top offer the highest performance solutions, targeting the highest end applications with the most stringent requirements.

Integrated LDOs Reduce Noise and Improve Performance

In addition to the MultiSynth architecture, clock generators include multiple features that contribute to low jitter and save system cost. For example, noise on the power supply is a significant problem in high-performance clock devices. It affects the performance in two ways:

1. It adds noise to the clock signal voltage and internal voltage references. Since crossing-point times are referenced to an internally-generated threshold voltage, this voltage noise will appear in the output as a timing error.
2. The power-supply noise is modulated by the internal oscillator in the PLL and contributes to phase noise.

Power supplies based on switching topologies are the preferred choice in high-current, low-voltage designs because they are highly efficient. Unfortunately, they also generate significant noise, so FPGA system designers must add low-noise low-dropout (LDO) linear regulators, ferrite beads, and numerous filter capacitors to remove power-supply noise before it reaches the clock generator. This adds significant cost and increases the board size.

Silicon Labs devices include multiple LDOs on the chip to largely eliminate the need for these external components.

The power supply to the output buffer circuits are regulated by independent internal LDOs that isolate the clock output buffer circuit from the noise on the power supply pins. The power supplies to internal digital, input buffer and analog circuitry also have independent internal voltage regulator circuits that isolate the internal oscillator from external power-supply noise.

The power-supply noise rejection (PSNR) figure is the key datasheet parameter: the newest devices such as the Si5341A and the Si5332, discussed below, have a PSNR of -100 dBc at 25kHz and -91 dBc at 1 MHz.

As a result, these devices require only a pair of filter capacitors on each power pin, drastically decreasing the system cost and solution size. The Si5332, for example, requires only 18 capacitors; a competing device requires LDOs, capacitors, ferrite beads, diodes and resistors - more than 100 additional components.

In conjunction with the timing solutions products, Silicon Labs offers several software tools that help customers develop quick-turn, customized solutions.

ClockBuilder Pro (CBPro) is a software tool that simplifies the task of getting from a clock-tree specification to an orderable part. CBPro supports Silicon Labs' Si539x, Si5121x, Si5350/1, Si5338, Si5332, Si534x, Si538x, and Si539x clock generators and jitter attenuators.

The tool uses a step-by-step GUI format that includes more than 175 clock design rules to reduce design and debug time. A built-in clock placement wizard assigns individual clocks to specific outputs to minimize the potential for

crosstalk. After configuring the part, customized performance reports complete with phase-noise plots are immediately available.

The software supports direct connection to all related EVBs and the CBPro Field Programmer. CBPro also supports in-system programming, allowing a system host to reconfigure the device while it is on the system board.

The CBPro software package is freely available for download. It includes the application executable file, Release notes, CLI (Command Line Interface) documentation, and general training information.

Other software tools include a phase noise- to-jitter **calculator** that helps translate FPGA phase noise specifications into jitter requirements.

Example of a Typical Design Flow

Developing a reference clock design consists of the following steps:

1. Define the clock tree: the frequencies, jitter performance, output signal levels, and other parameters related to the timing requirements
2. Based on that set of requirements, select the clock generator that aligns with the jitter performance requirement and number of outputs
3. Use ClockBuilder Pro to input the clock tree requirements and create a configuration file
4. ClockBuilder Pro will assign a unique/custom part number (-xxxxxx suffix) corresponding to the configuration file developed. It will also provide a datasheet addendum to the customer.
5. The part number with its associated configuration file is automatically generated in the Silicon Labs backend system
6. Samples or production-quantity parts can be ordered immediately; these are shipped within 2 weeks of the order being received.

Design Example with Intel Stratix 10

Here is a design example using the default frequencies in the Intel® Stratix® 10 GX FPGA Development Kit. The Stratix 10 is Intel's highest performance FPGA family; the Stratix 10 GX achieves up to 10 TFLOPS with transceiver support up to 2.8 Gbps.

There are fifteen reference clocks called out in the Stratix Development kit, shown in the table below. These range from 50 MHz to 644.53125 MHz and fulfill a variety of roles: system clocks for the Stratix 10 FPGA and the MAX V CPLD (Complex Programmable Logic Device, a lower-cost, simpler FPGA variant); and reference clocks for common communication standards such as Ethernet, DisplayPort, and the high-speed transceivers.

Device	Clock	Frequency (MHz)	Level	Function
Si5341A	REFCLK1	155.52	LVDS	Transceiver ref. clock Bank 1D
Si5341A	REFCLK_QSFPI1	644.53125	LVDS	QSFP ref. clock
Si5341A	REFCLK_DP	135	LVDS	DisplayPort ref. clock
Si5341A	REFCLK4	156.25	LVDS	Transceiver ref. clock Bank 4E
Si5341A	REFCLK_FMCA	625	LVDS	FMC ref. clock
Si5341A	FPGA_OSC_CLK1	125	LVCMOS	FPGA configuration clock
Si5341A	CLK_ENET	125	LVDS	Ethernet clock
Si5341A	MAXV_OSC_CLK1	125	LVCMOS	MAX V CPLD clock
Si5341A	CLK_CONFIG	125	LVCMOS	MAX V CPLD clock
Si5332	CLK_MAXV_50M	50	LVCMOS	MAX V CPLD clock
Si5332	CLK_FPGA_50M	50	LVCMOS	FPGA clock
Si5332	PCIE_OB_REFCLK	100	LVDS	Onboard PCIe ref. clk
Si5332	CLK_HILO	133	LVDS	HiLo memory clock
Si5332	CLK_FPGA_B3L	100	LVDS	FPGA clock Bank 3L
Si5332	REFCLK_SDI	148.5	LVDS	SDI ref. clock

These clocks can be supplied by only two Silicon Labs clock generators, as shown below:

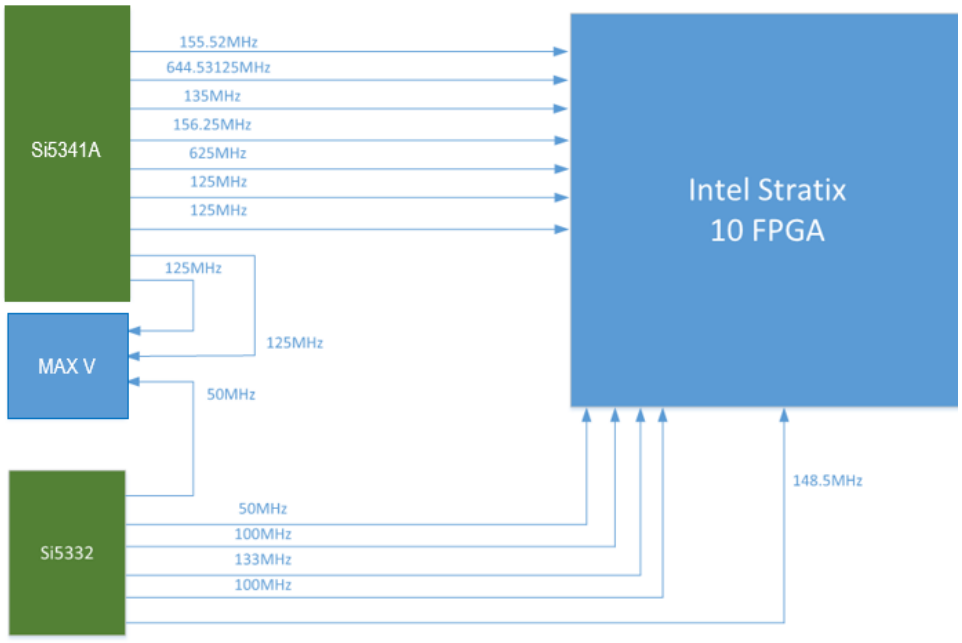


Figure 5: Two Silicon Labs clock generators can supply all default clocks for the Intel Stratix 10 Development Kit

The Si5341A and Si5332 are used in this design. Why were these parts selected?

- They meet the maximum jitter performance requirements in the Intel Stratix FPGA specification for all reference clocks, with sufficient margin.
- They consolidate the clock frequencies into only two clock generators. This minimizes PCB footprint and number of components, reducing cost.
- They provide additional features like output enable pins, spread spectrum for EMI reduction, frequency control/selection

The Si5341 (figure 6) provides ten outputs: frequencies range from 100 Hz – 1028 MHz for differential outputs or 100 Hz – 250 MHz for LVCMOS levels with jitter of only 90 fs RMS. Either a crystal or an external differential input can supply the input frequency. The outputs are configurable to meet LVDS, LPECL, LVCMOS, CML, and HCSL specifications.

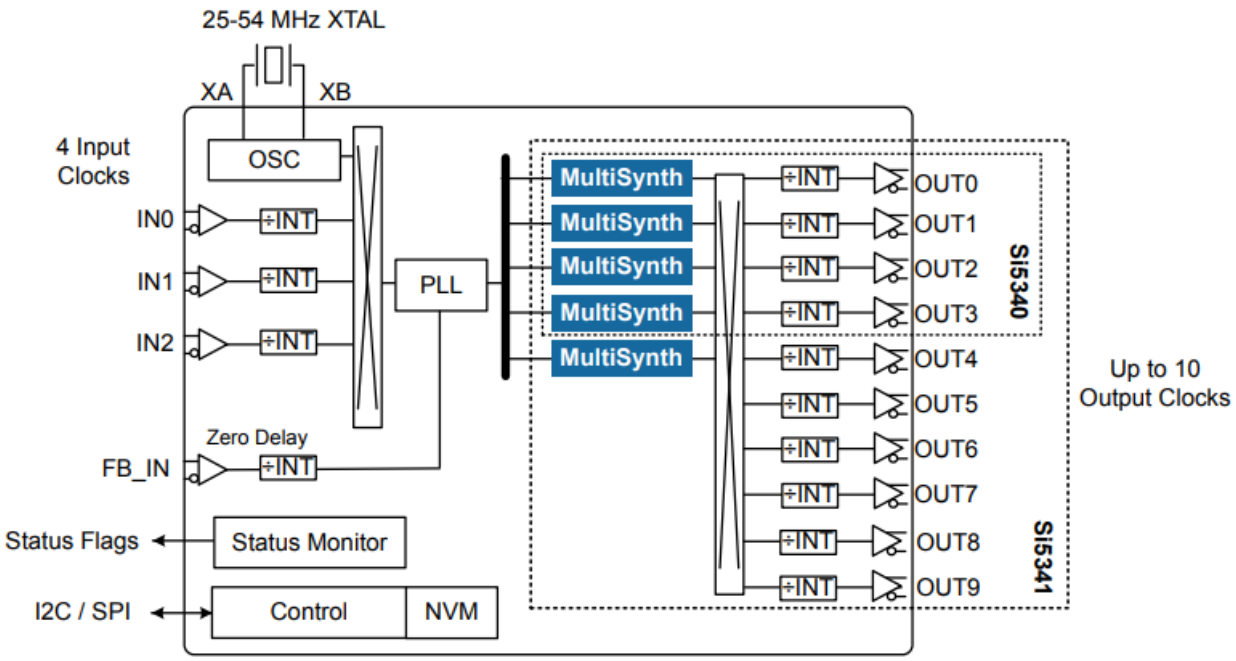


Figure 6: The Si5341 generates ten independent reference clocks

The remaining five outputs are courtesy of the Si5332. This device comes with six, eight, or twelve outputs. The output clocks can reach up to 333.33 MHz differential and 170 MHz LVCMOS with phase jitter as low as 175 fs RMS, more than enough for the application. The Si5332 is also available with an embedded crystal that further reduces cost and size.

Conclusion

Designing a reference clock tree for a high-performance FPGA design is an exacting task, but Silicon Labs' portfolio of clock generators offers a flexible and powerful way to meet these stringent requirements. Together with the ClockBuilder Pro software tool, designers can now develop an optimum solution and quickly evaluate sample parts.